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Research Paper

Sequential Nitrogen Ion Implantation in Si-Based GaAs Matrix and Subsequent Thermal Annealing Process: Electrical Characterization

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The ion implantation is well-established techniques for device fabrication in III-V semiconductors. GaAs is grown on Silicon (Si) substrate using Germanium (Ge) as a buffer layer to reduce the lattice mismatch. The implantation of nitrogen ions in GaAs layers of the epitaxial-grown structure GaAs/Ge/Si is done with sequential implantation of doses from 0.8 x 10^{17} to 2.0 x 10^{17} cm^{-2} with respective energies ranging from 40 keV to 120 keV per atomic ion. This was aimed to achieve more uniform depth distribution of nitrogen as a result of multiple ion implantation. A subsequent high temperature annealing is done for nanostructures formation and to improve the crystal quality. For the annealing process, rapid thermal annealing (RTA) and furnace annealing (FA) are used in temperature range of 700°C-850°C under argon and nitrogen environment. Current-voltage (I-V) characterization are carried out to study the effect of the post-annealing process on the barrier height and ideality factor. The electrical parameters are observed to have a strong dependence on temperature. The inhomogeneity in barrier height gives rise to the temperature dependence of barrier height.

Keywords: Gallium Arsenide; Ion Implantation; Annealing; Optical Lithography; Barrier Height

Introduction

The direct ion implantation technique is widely used to modify optical and electrical properties of III-V based compound semiconductors (Pearton 1990). The requirement of precise doping profile, distribution of implanted species and reproducibility makes the ion implantation a standard non-destructive process (He *et al*., 1991). Nowadays nanostructures are going under extensive research by several groups in order to use them in several optoelectronic applications. Semiconductor nanostructures can be grown on various substrates by several techniques such as molecular beam epitaxy, metalorganic chemical vapour deposition and chemical routes. Gallium nitride (GaN) is used for a wide range of applications like light emitting diodes, laser, and power electronics devices due to its excellent optoelectronic properties (Nakamura *et al*., 1996; Morkoc *et al*.). However, the growth of GaN and gallium arsenide (GaAs) is still a difficult task due to their lattice and thermal expansion coefficient mismatch with CMOS compatible materials like Si (Kroemer 1986). The fabrication of nanostructures embedded in a GaAs matrix is quite interesting for realizing the modern devices due to high mobility and the direct bandgap of GaAs, but it is a challenging task. Ion implantation is an appropriate method by which the embedded nanostructures can be formed inside the matrix (Lin *et al*., 1995 and Wolk *et al*., 1997). Ion implantation technique is also compatible with semiconductor nanotechnology and can be used to modify optical and electrical characteristics of semiconductor materials. Unlike the conventional thin films or nanocrystals on a substrate, this method provides encapsulation and passivation, as the nanocrystals are formed directly in a substrate matrix. Another advantage of this technique is the ability to control the concentration, size and localization of the implanted

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species, which allows tailoring optical, electrical and magnetic properties.

The ion-implantation in the GaAs matrix have been carried out by many researchers to modify their optical and electrical properties. The N ion implantation in the GaAs matrix is the most suitable process to form GaN based nanostructures for high temperature and high-power devices due to their excellent thermal stability. The device based on ion-synthesized nanostructures provides an innovative approach for realizing photodetectors (Koo *et al*., 2006; Rajamani *et al*., 2018). In the GaAs matrix, the direct bandgap and high mobility allow producing integrated optoelectronic devices. Although there is very large mismatch between lattice constant of GaAs and GaN (20%), it has been found that the GaN nanostructures could be formed in GaAs matrix by implantation of N_1^+, N_2^+ ions and thermal annealing (De Luise, 1993; Lin *et al*., 1995; Wolk *et al*., 1997; Amine *et al*., 2002; Weng *et al*., 2005a). In such cases, high temperature annealing enhances the exchange interaction between N and As atoms in the GaAs matrix which is thermodynamically favourable (Lin *et al*., 1995; Amine *et al*., 2002). Also, we know that As is more volatile than Ga which also facilitates the As replacement by N under implantation followed by the annealing process. And the other aspect is that the ion-implantation technique is beyond the solid solubility limits (Lin *et al*., 1995). The optical studies also reveal the formation of GaN based nanostructures in GaAs matrix by ion implantation (Weng *et al*., 2002b; Bumai *et al*., 2005).

In this work, we present the implantation of nitrogen ions in the Si-based GaAs layer obtained by an original approach (Buzynin *et al*., 2017) that combines different epitaxial techniques to produce high-quality hybrid Si/Ge/GaAs structures to be used instead of GaAs monolithic substrates for fabrication of solar cells, photodetectors, LEDs, lasers, etc. This method of synthesis of GaN nanocrystals in GaAs matrix is of extra interest because, on the one hand, it is compatible with silicon technology and, on the other hand, it provides ample opportunities for advanced micro and optoelectronic devices due to the creation of nano (hetero) compositions from four materials – Si, Ge, GaAs and GaN. Compared to the case of ion synthesis of GaN nanocrystals by co-implantation (Ga^+ and N^+) into SiO_2/Si (Korolev *et al*., 2017) the present method is simpler from the technological point of view and excludes the problem of out-diffusion of implanted atoms during annealing (Lin *et al*., 1995; Amine *et al*., 2002; Bumai *et al*., 2005). The I-V characterization is studied to see the effect of ion-implantation in the GaAs matrix in terms of implantation doses and annealing conditions. Figure 1 shows the schematic process of the ion implantation in GaAs and nanostructure formation.

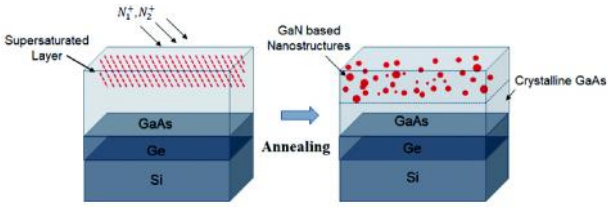

Fig. 1: Schematics of the ion-implantation and nanostructure formation in the Si-based GaAs matrix

Materials and Methods

After growth of 100 nm p-Si on n-Si substrate by molecular-beam epitaxy, a 600 nm Ge layer was grown by the hot-wire chemical vapour deposition technique at 300°C. After that, a 1000 nm thick GaAs layer was grown by metal-organic chemical vapour deposition. Detailed information about the complete technological route and quality of epitaxial layers can be found elsewhere (Buzynin *et al*., 2017). A chemical cleaning of n-Si/Ge/GaAs substrate is done prior to the ion implantation. The sequential ion implantation of N_1^+ (120 keV and 80 KeV) and N_2^+ (80 keV) was done using ILU-200 (Russia) ion implanter at the pressure lower than 10^{-6} Torr in the target chamber (maintained by the oil-free pumping). Molecular N_2^+ ions were used to reduce the irradiation time: as the N_2^+ molecular ion at the first collision breaks up into two atomic ions with equal energies, such irradiation is equivalent to that of atomic beam with a doubled dose at half the energy. The sequential implantation was performed in order to get more homogeneous depth profile of implanted atoms in GaAs layer according to the SRIM simulation (Fig. 2).

After the implantation, the samples are processed for thermal annealing by rapid thermal annealing (RTA) in an argon atmosphere for 30 sec or furnace annealing (FA) in the nitrogen atmosphere for 15 minutes. The JIPELEC JetFirst 100 system is

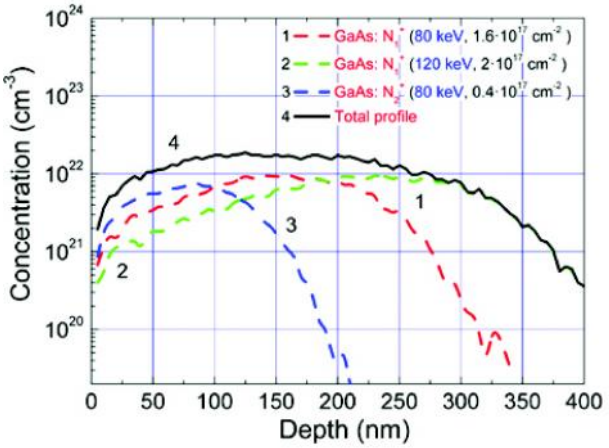

Fig. 2: SRIM-simulated depth profiles of implanted ions

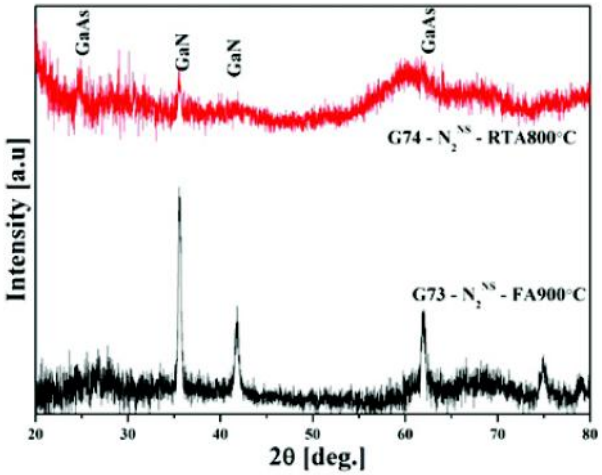

Fig. 3: XRD patterns for the samples of GaAs implanted with N_2^+ (40 keV, 2.5'·10^{16} cm^{-2}) and subjected to RTA and FA treatments

used for RTA treatment. For references, sample series 0 is characterized where only annealing step is done. The sample series 1, where ion implantation and annealing are done, is listed in Table 2 with detailed parameters. The ion beam current density is kept constant at around 7 μA/cm^2 for sample series 1. During thermal annealing, a proximity method is used where the implanted side is covered with GaAs wafer to reduce the arsenic evaporation from the surface.

The formation of GaN nanocrystals in ion-implanted samples after RTA and FA is confirmed by the X-ray diffraction (XRD) data obtained for the reference bulk GaAs samples (Fig. 3). According to the physical arguments, one can be aware that these results could be transferred to the samples used for electrical measurements.

The samples were further processed for device fabrication, where Cr(10 nm)/Au(200 nm) thin films are deposited by thermal evaporation to fabricate interdigitated electrodes (IDEs). The IDEs are defined using a standard photolithography process. The IDEs forms back to back Schottky contacts. The pattern provides 30 μm gapes between the fingers and

Table 1: Details of samples for series 0

Sample series 0	Annealing	Time
00	as grown	————
01	RTA (800°C)	30 sec
02	FA (700°C)	15 min
03	FA (800°C)	15 min
04	FA (850°C)	15 min

provides an effective length of electrodes around 1 mm. Figure 4(A-E) shows the schematic representation of the fabrication IDEs of Cr/Au on GaAs by thermal deposition and lithography process. Figure 4(F) shows the optical micrograph of IDE. The current-voltage (I-V) characteristic of the structures is measured by Keithley SCS 4200 on a probe station.

Results and Discussion

The growth of GaAs on Ge is always associated with defects due to lattice mismatch and difference in

Table 2. Details of ion implantation and annealing parameters of samples for series 1

Samples series 1	N_1^+(E=120 ke V, j=7μA/cm^2)	N_1^+(E=80 ke V, j=7μA/cm^2)	N_2^+(E=80 ke V, j=7μA/cm^2)	Annealing
11	2×10^{17} cm^{-2}	$1.6\times10^{17}$$cm^{-2}$	$0.4\times10^{17}$$cm^{-2}$(atomic dose $0.8\times10^{17}$$cm^{-2}$)	RTA (800°C, 30s)
12	2×10^{17} cm^{-2}	$1.6\times10^{17}$$cm^{-2}$	$0.4\times10^{17}$$cm^{-2}$	FA (700°C, 15min)
13	2×10^{17} cm^{-2}	$1.6\cdot10^{17}$$cm^{-2}$	$0.4\times10^{17}$$cm^{-2}$	FA (800°C, 15min)
14	2×10^{17} cm^{-2}	$1.6\times10^{17}$$cm^{-2}$	$0.4\times10^{17}$$cm^{-2}$	FA (850°C, 15min)

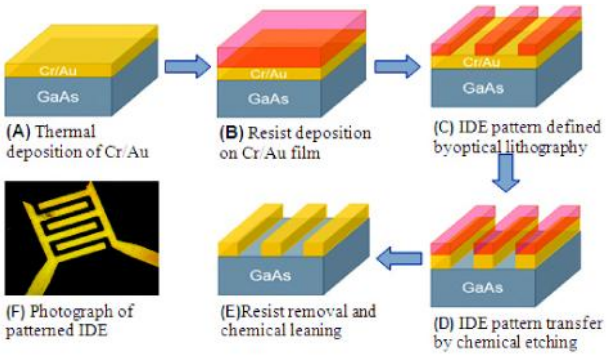

Fig. 4: (A-E) Show the fabrication process of integrated electrodes on the GaAs wafer. (F) shows the optical micrograph of patterned IDE. There is 30 µm gap between the IDE fingures

thermal expansion coefficients (Petroff, 1986). The annealing step is mostly used to improve the crystalline quality of the layer after heteroepitaxial growth.

Figure 5(A) shows the current-voltage characteristic of the series-0 where only annealing step is processed. The nonlinear and symmetric I-V curve suggests the back to back Schottky contacts between GaAs and Au electrodes. Here we observe that the current in the RTA sample (01) increases to three orders of magnitude compared to the as-grown sample (00). The larger value of current in annealed samples is due to the reduction of defect concentration and improvement of crystalline quality of the GaAs layer grown on Ge.

Figure 5(b) shows the I-V characteristics of the series 1 where nitrogen implantation is followed by annealing step. The lower currents in these samples compared to series 0 is attributed as due to the ion-beam damage of the GaAs matrix, which reduces the concentration and mobility of charge carriers. The incorporation of nitrogen into the GaAs also reduces the mobility of the carriers (Duncan and Matteson, 1984). The other assumption is that the formation of GaN nanocrystals after annealing lowers the carrier mobility in GaAs matrix but do not contribute to the electrical conduction.

The rectifying behaviour of the I-V characteristic for the metal-semiconductor junction is dominated by thermionic emission and is expressed by the following equation (Sze 1981, page 256):

$$I = I_s\left[\exp\left\{\frac{qV}{\eta kT}\right\} - 1\right] \text{ with}$$

$$I_s = AA^*T^2 \exp\left(-\frac{\phi_b}{kT}\right), \qquad (1)$$

where I_s is the saturation current, q is the elementary charge, V is the applied voltage, η is the ideality factor, Φ_b is the barrier height, k is the Boltzmann constant, A is the contact area, T is temperature in Kelvin scale and A^* is the Richardson constant. For different barrier heights in a metal/semiconductor/metal junctions, the back to back Schottky contacts show rectifying behaviour where the current is dictated by the reverse biased junction. In such conditions, the current can

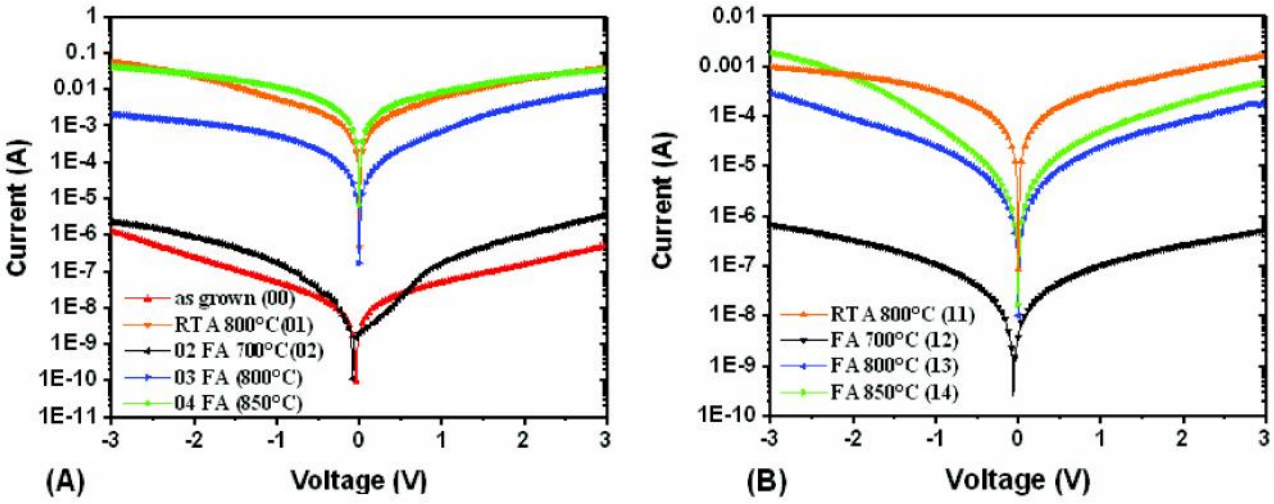

Fig. 5: (A) shows I-V curve of annealed GaAs samples for series 0 and (B) shows the I-V curve of nitrogen ion implanted GaAs samples of series 1

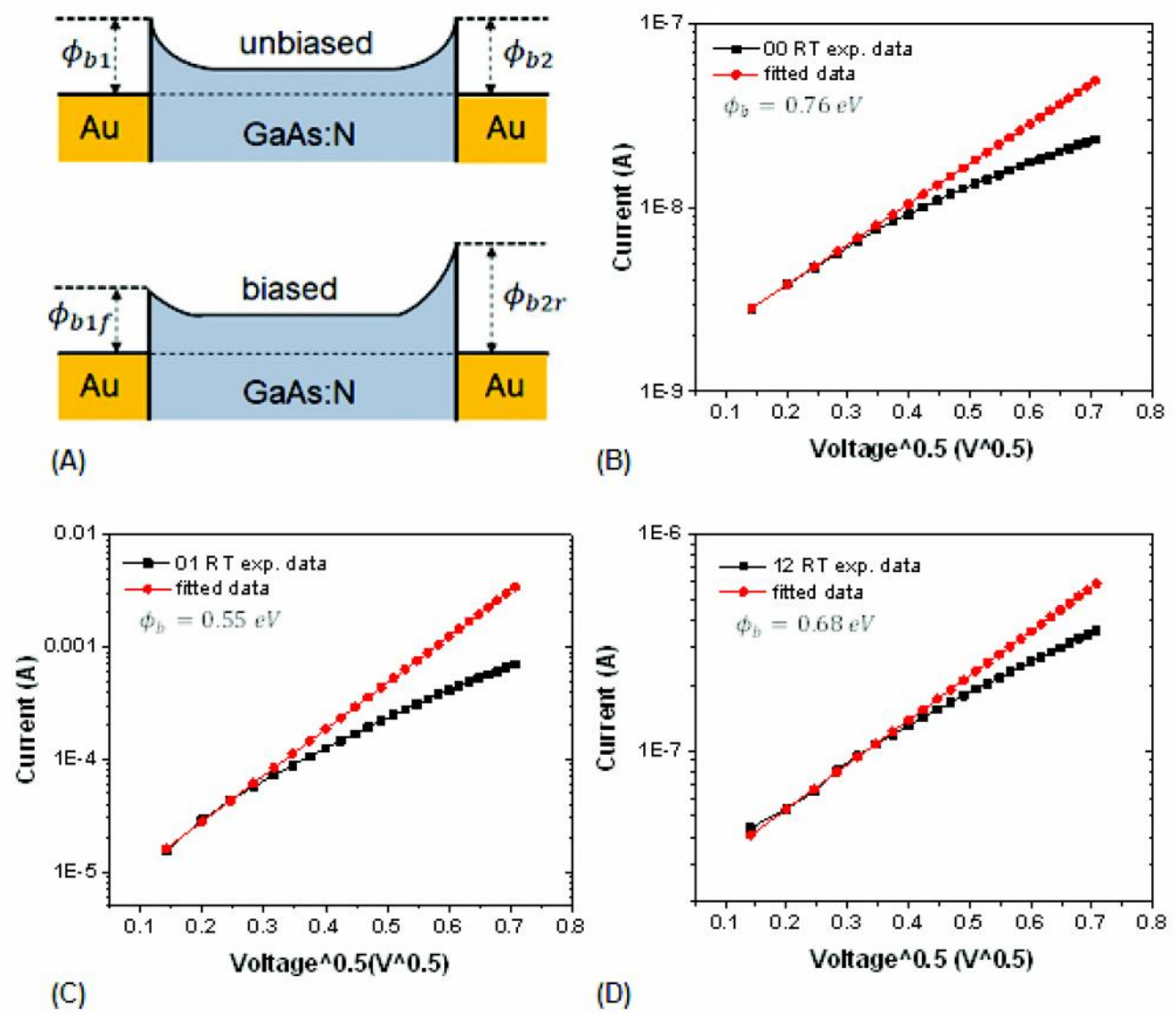

Fig. 6: (A) shows the schematic of the energy band diagram for unbiased and biased Schottky contacts and (B), (C), and (D) show room temperature I-V curve for different samples fitted with Bardeen model to calculate the barrier height

Table 3: Calculated barrier heights for different samples by Bardeen model

Sample series 0 unimplanted	Barrier height (eV)	Sample series 1 implanted	Barrier height (eV)
00 (as grown)	0.76	————	————
01 (RTA 800°C)	0.55	11 (RTA 800°C)	0.65
02 (FA, 700°C)	0.75	12 (FA, 700°C)	0.68
03 (FA, 800°C)	0.58	13 (FA, 800°C)	0.73

be expressed by Bardeen model (Zhang and Harrell, 2003; Ranwa *et al.*, 2014).

$$I = I_0 \exp\left(\frac{\beta\sqrt{V}}{kT}\right) \tag{2}$$

where I_0 is the reverse saturation current, β is the interface related parameter, k is the Boltzmann constant, V is the applied bias and T is the absolute temperature. The I_0 is related to barrier height (Φ_b) by the equation:

$$I_0 = AA^*T^2 \exp\left(\frac{-q\phi_b}{kT}\right) \tag{3}$$

where A* is the Richardson constant. The Richardson

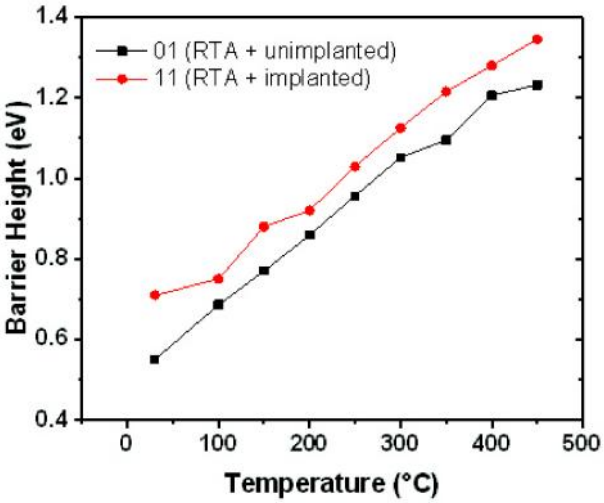

Fig. 7: Temperature dependent barrier height variation for unimplanted and implanted GaAs samples

constant for p-GaAs is approximately 75 A-cm^{-2}-K^{-2}. Exponential fitting is used to calculate the barrier using equation

$$I = a\exp\left(b\sqrt{V}\right) \quad (4)$$

where a is defined as I_0 and used to calculate the barrier height. The barrier height is calculated in low voltage regime because at higher voltages the current quickly becomes dominated by series resistance and deviates from linearity. Figure 6(A) shows the schematic representation of the energy band diagram for metal/semiconductor/metal junction under unbiased and biased conditions. Figures 6(B), (C), and (D) show the fitting according to equation 4 to calculate the barrier height of the Schottky junctions.The barrier height for as-grown GaAs sample (00) is higher compared to RTA annealed sample which is due to improved crystalline quality and reduced surface states. A similar effect is also observed in the ion implanted samples. The implantation process damages the surface and creates surface defects which increase the barrier height as seen in Fig. 6(D). Table 3 shows the barrier height of different samples calculated by Bardeen model. As-grown GaAs on Si shows very high barrier height (S 0.76 eV) which is due to low crystalline quality of GaAs. After RTA, the barrier height is reduced to the 0.55 eV which is lower than the ideal value. The lower barrier height is attributed to the oxide formation during the annealing process (Sharma *et al*., 2007). Here we also oserved that the barrier height of the unimplanted FA @ 700°C GaAs sample (01) has similar value to as-grown GaAs sample (01). This implies that FA at 700°C does not improve the crystalline quality of as-grown GaAs. Sometimes at high temperature furnace annealing (S 800°C or above), due to arsenic eveporation from GaAs surface, increases the surface roughfness and increases the barrier height as observed in the sample (13). The ion implantation also changes the Schottky barrier height (Baranwal *et al*., 2009). The ion implantation induces damage at the surface which results in the higher barrier for the contacts as seen in the sample (11).

The temperature dependent study of the barrier height is done for the unimplanted and implanted GaAs samples as shown in Fig. 7. The current transport in the metal-semiconductor junction is a temperature dependent process where the electrons are transported through low barrier at low temperatures and high barrier at high temperatures. At low temperature, the carriers surmount the low barrier and transport take place through lower barrier paths. Similarly as the temperatures increases, carriers get sufficient energy to overcome the higher barrier. Therefore the barrier height increases with increasing temperature (Mahato *et al*., 2017).

In conclusion, sequential implantation of nitrogen ions into GaAs followed by thermal annealing has been performed. The I-V characteristic is performed to see the effect of annealing and nitrogen ion implantation in GaAs. The annealing process after ion implantation forms the GaN nanostructures and improves the crystalline quality. The experimental results show that the Schottky barrier height for metal-semiconductor junction depends on the growth parameters and post-annealing process. The increase in barrier height at Au (Cr)/GaAs contacts in implanted samples is due to ion beam damage at a surface and amorphization of GaAs.

Acknowledgements

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